Raman and Photocurrent Imaging of Electrical Stress-Induced p–n Junctions in Graphene

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ABSTRACT Electrostatically doped graphene p–n junctions can be formed by applying large source–drain and source–gate biases to a graphene field-effect transistor, which results in trapped charges in part of the channel gate oxide. We measure the temperature distribution *in situ* during the electrical stress and characterize the resulting p–n junctions by Raman spectroscopy and photocurrent microscopy. Doping levels, the size of the doped graphene segments, and the abruptness of the p–n junctions are all extracted. Additional voltage probes can limit the length of the doped segments by acting as heat sinks. The spatial location of the identified potential steps coincides with the position where a photocurrent is generated, confirming the creation of p–n junctions.

KEYWORDS: graphene · electronic · Raman · photocurrent · electrical stress

Graphene, a layer of carbon atoms arranged in a 2D hexagonal lattice, has created much interest in nanoelectronic research since it was isolated in 2004.[1] Its charge carriers behave like massless Dirac fermions exhibiting linear dispersion, zero band gap, and high carrier mobilities.[2–4] The planar nature of graphene and recently demonstrated wafer-scale production[5,6] make it an attractive candidate for post-CMOS device fabrication, as it can be easily integrated into current CMOS device processing. Because single-layer graphene is a zero-band-gap semiconductor, it is not suited for digital applications, and graphene p–n junctions are, in contrast to traditional diodes, not rectifying. However, graphene supports modest current modulation due to its low density of states near the Dirac or charge-neutrality point (CNP), and graphene p–n junctions may offer applications beyond current technology, such as Klein tunneling,[7,8] where electrons traveling perpendicular to the junction experience zero resistance, or Veselago lensing,[9] where diverging electron waves are refocused by the junction. Earlier work on graphene p–n junctions focused on multiple electrostatic gates or chemical doping, in which the junction is formed by using top and bottom gates[10–12] or chemical modifications on top of the graphene.[13,14] An approach that does not involve use of multiple gates or additional lithography but creates the junction by controlling the local electrostatic potential along the channel was demonstrated recently.[15] By applying large gate and drain voltages, charges were trapped near the gate oxide surface, exclusively at the drain side of the device. The modification of the electrostatic potential reveals itself by a second CNP in the gate-voltage characteristics, suggesting that the device consists of two graphene channels with different Dirac points in series, thus forming a junction. Here we use Raman spectroscopy to characterize the thermal conditions during the electrical stress and extract the electrical stress-induced doping profile along the device. We find that a p–n junction is indeed formed, which can act as a photodetector. The Raman method locates the p–n junction, measures the abruptness of the junction, and determines absolute doping levels. Additional photocurrent measurements on multiple-junction devices, produced by multiple electrical stresses, show that the photosensitive area jumps from junction to junction as the Fermi level is swept by the backgate.

Our graphene p–n junctions are formed by applying high gate and drain voltages and trapping charge carriers in part of the oxide surface or immediate subsurface.[15] Details of the electrical stress procedure are given in the Methods section. An effective gate voltage V_G of (i) $V_G - V_{CNP} < V_D < 0$ V during the electrical stress facilitates p-type transport and hole trapping, whereas (ii) $V_G - V_{CNP} > V_D > 0$ V favors n-type transport and electron trapping. Here V_D is the drain

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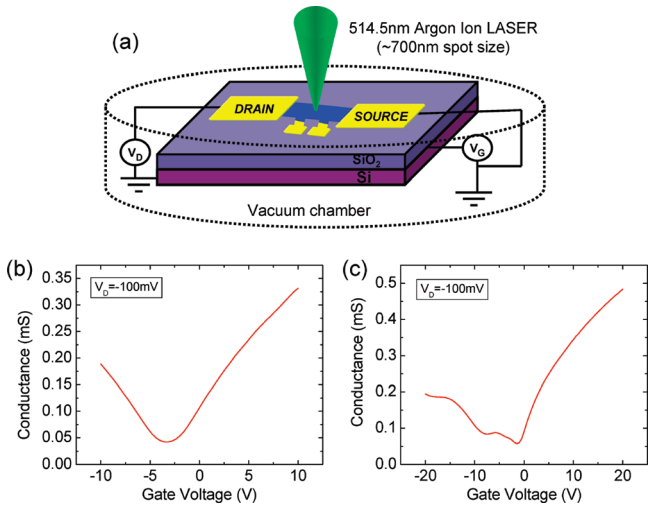

Figure 1. Sample and setup. (a) Schematic illustration of the vacuum sample stage with focused laser light of λ = 514.5 nm incident on the graphene backgated device. The outline of the graphene is shown in blue, and the contacts are yellow. (b) Conductance plot of the device with single charge-neutrality point. After electrically stressing the graphene with $V_D = -10$ V and $V_G = -20$ V, it becomes locally doped, evident from the transfer curve measured subsequently (c), which shows secondary dips near −8 and −18 V. A small shift in the original charge-neutrality point from −3.5 to −1.5 V is laser-induced.

voltage and V_{CNP} is the voltage of the charge-neutrality point. Due to the high drain bias, either condition leads to a non-uniform charge density along the channel with fewer carriers near the biased contact.[16,17] The fewer carriers have to move faster to conserve the current, thus producing energetic holes (i) or electrons (ii) in the graphene channel near the biased contact. This in turn leads to hole (i) or electron (ii) trapping at or near the oxide surface near the biased contact. Figure 1b,c shows $G-V_G$ characteristic before and after such an electrical stress with $V_D = -10$ V and $V_G = -20$ V, leading to additional dips at negative gate voltages (here at −8 and −18 V) due to hole trapping near the biased contact. In ref 15, only hole trapping was achieved, while we now find that both carriers can be trapped using the appropriate conditions (i) or (ii). The difference is probably due to the history of the wafers since the trapping happens close to the surface and different surface treatments, extended exposure to air, the duration, and temperature of the sample bake-out, trapped species between the graphene and SiO_2, *etc.*, all can affect the density of surface and near-surface states for electron and hole trapping. From a theoretical point of view, electron and hole trapping should be entirely analogous, as long as the corresponding trap states are available.

The most prominent Raman features of graphene are its G-peak around 1590 cm^{-1} and 2D-peak around 2700 cm^{-1}. The G-peak corresponds to a phonon at the Brillouin zone center,[18] while the 2D-peak involves two zone-boundary D-band phonons. The 2D shape distinguishes single and multilayer samples.[18] Raman spectroscopy has been a useful and robust tool for monitoring doping,[19−21] identifying layer numbers,[18] defect identification,[22,23] and temperature measurements.[16,24,25] The effect of gating on the G-band was reported in refs 19 and 20. The frequency of the G-band increases, and its full width at half-maximum (fwhm) decreases for both electron and hole doping. The stiffening of the G-peak is due to the nonadiabatic removal of the Kohn anomaly. The fwhm sharpening is due to blockage of the phonon decay into electron−hole pairs due to Pauli exclusion when the Fermi level becomes higher than half the phonon energy. The 2D-peak is also affected by doping,[19] albeit to a lesser extend than the G-peak. Thus G-band maps best depict the p−n junction formation by modification of the local electrostatic potential. We use our own calibration of the Raman bands as a function of electrostatic gating, performed on a sample that was later employed for the electrical stress experiments (see Supporting Information). Both G- and 2D-bands are also susceptible to temperature due to the anharmonic coupling of the G and D phonons to intermediate frequency and acoustic phonons. The phonon softening rates with temperature have been measured for both phonons.[25] The 2D shift with temperature is larger (−0.034 cm^{-1}/K) than the G-peak shift (−0.016 cm^{-1}/K) mainly because it involves two phonons, and thus we use the 2D shift to measure the temperature *in situ* during the electrical stress. Doping effects can be excluded by using the frequency of the 2D-band at zero drain bias as the baseline for the temperature measurements (room temperature).

We first focus on the doping profiles of the graphene p-n junctions. Figure 2a shows the Raman G-band as a function of position along the graphene device after different stages of electrical stress. In (ii), the device is in its original state and the G-band frequency around 1586 cm^{-1} is close to uniform throughout the device. Slight differences in the G-band frequency can be attributed to pre-existing dopants or electron−hole puddles that were not completely removed during the pumping/outgassing of the device.[26] In (iii), an

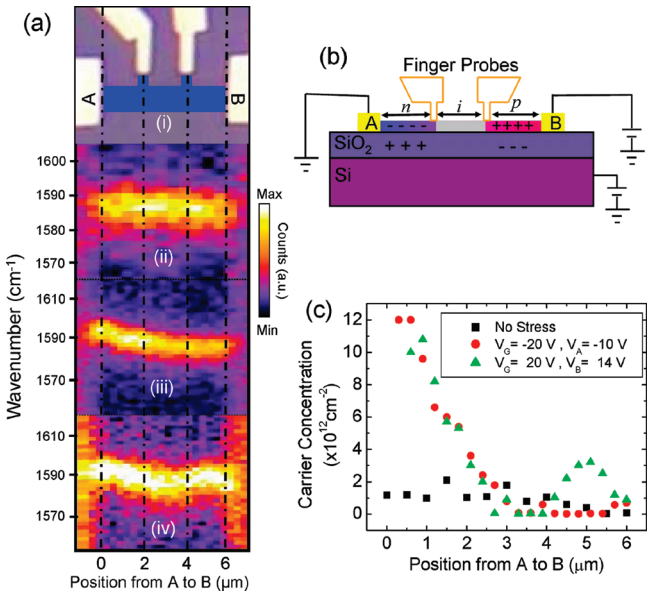

Figure 2. Doping profile in electrically stressed graphene. (a) Raman G-band mapping of the graphene field-effect transistor. (i) Optical image of the graphene device showing metal contacts (A and B) and two intermediate metal contacts that were left floating. (ii–iv) Intensity of the Raman scattered light (color coded) as a function of position from A to B (*x*-axis) and wavenumber (*y*-axis) (ii) without any electrical stress; (iii) after electrical stress of the left side with $V_A = -10$ V and $V_G = -20$ V; (iv) after additional electrical stress of the right side with $V_B = 14$ V and $V_G = 20$ V. The G-band stiffens near contact A due to trapped holes in the oxide that were deposited during stress (iii) and additionally near contact B due to trapped electrons deposited during stress (iv). (b) Schematic of the device at stage (iv) showing trapped charges in the SiO_2 creating mirror charges in the graphene channel close to the contacts. (c) Carrier concentration along the channel, extracted using the Raman calibration and the measured G-peak frequency along the channel, both shown in the Supporting Information.

electrical stress of up to $V_A = -10$ V at contact A and a gate voltage of $V_G = -20$ V leads to a strong stiffening of the G-band near the biased contact after the electrical stress is removed. We can understand the G-band stiffening by the trapping of holes in the SiO_2 close to the biased contact. These trapped holes induce mirror charges (electrons) in the graphene, thus producing an n-type segment in the unbiased graphene close to contact A. From the G-band frequency and the calibration between n and G-band frequency (see Supporting Information), we can extract a density of $n = 10^{13}$ cm^{-2} in the immediate vicinity of contact A, a density of $n \sim 5 \times 10^{12}$ cm^{-2} further along the channel, and a density below $n = 10^{12}$ cm^{-2} on the other side of the device (see Figure 2c). In (iv), we trapped electrons on the other side of the device, using $V_G = 20$ V and $V_B = 14$ V at the contact B. The positive gate voltage leads to electron transport during the electrical stress, and the positive voltage at contact B leads to hot electrons in the graphene near that contact. Some of these hot electrons are trapped in the oxide near contact B and lead to p-type doping in that segment. A schematic cross section of the n–i–p junction thus formed is shown in Figure 2b. Indeed, we find that the Raman G-band now indicates a density of 3×10^{12} cm^{-2} holes in the graphene, due to the trapped electrons near contact B (green triangles).

Upon closer inspection of the extracted carrier concentration in (iv), one can see that the doping extends from the contacts about 2 μm to the nearest finger probes, but the area between the two finger probes remains undoped. Note that these plots are broadened by the finite laser spot size of about 700 nm so the physical widths of the n–i and i–p junctions can be calculated to be only a few 100 nm. On the left side, there exists a strongly doped segment right at contact A, created during stress (iii), in addition to the more lightly doped part extending to the finger probe. This is consistent with the $I-V_G$ in Figure 1c that was taken after the electrical stress leading to (iii) and which shows two additional CNPs at −8 and −18 V instead of only one additional CNP at −8 V. The strongly doped segment right at contact A arises from additional, uncontrolled charge injection near the contact during the electrical stress. On the right side, such a contact-induced effect is absent, which is what we most often see. In fact, there is reduced doping near contact B because the temperature during the stress is lower in the first few 100 nm of the graphene due to heat sinking by the contact.[27] The extent of the doped segments (2 μm) is slightly more than the 1 μm estimate from ref 15 that was based purely on electrical measurements. This can be explained partly by the electrical contribution of intrinsic graphene regions in contact with electrodes that act as heat sinks. After studying many junctions, we have found that finger probes tend to limit the extent of the doping, even if they only contact the channel from one side with an extended graphene section. Near a contact, there may be additional complications, such as charge trapping

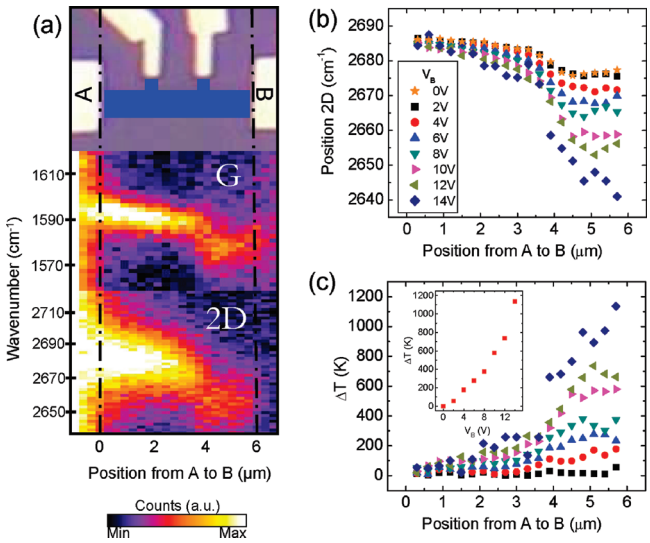

Figure 3. Temperature distribution in a graphene field-effect transistor during electrical stress. (a) *In situ* Raman G-band and 2D-band spatial mapping during electrical stress with bias of V_B = 10 V and V_G = 20 V. The color-coded Raman intensity is plotted as a function of position (*x*-axis) and wavenumber (*y*-axis). The area between contact B and the finger electrode exhibits strong phonon softening because of the high temperatures there. The sample is kept at room temperature during the experiment. (b) Extracted frequency of the 2D-peak as a function of spatial position for V_G = 20 V and V_B = 0 V to 14 V as indicated. (c) Extracted temperature increase above room temperature in the device during the electrical stress, peaking at about $\Delta T \sim$ 1000 K in the segment between contact B and the finger electrode. Inset: temperature increase near contact B.

associated with the contacts themselves, or heat sinking by the contact. If voltages are stepped carefully, the extent of the doping into the channel may be limited by the applied voltages rather than finger probes. However, in devices without finger electrodes, there is a delicate balance between the highest drain and gate voltages that needs to be applied to push the doping far into the channel and the point where the boundary simply moves across the entire device, making it completely doped.

To better understand how the junctions are formed during the electrical stress, we monitor the graphene Raman lines *in situ* during repeated application of the same high bias voltages (Figure 3). Both the Raman G-band and 2D-band show strong phonon softening in the area between the biased contact B and the neighboring voltage probe. This is partially due to sample self-heating and partially due to electrostatic doping (the latter being a combination of electrostatic doping by the applied gate voltage, V_G = 20 V, and electrostatic doping by the trapped charges). Since the carrier density on the right side of the device is lower, current continuity requires that carriers near contact B move faster, and thus more power is dissipated locally near that contact. We can quantify the temperature during the electrical stress using the shift of the 2D-band[25] with increasing bias, compared to the V_B = 0 V, V_G = 20 V case (Figure 3c), which eliminates the electrostatic effects of the backgate and trapped charges. At 14 V bias, the temperature increase reaches more than 1000 K on the right side compared to only around ~100 K on the left side. This sharp drop in temperature over such a small distance is due to both the non-uniform power dissipation along the device and the heat-sinking properties of the finger gate. The inset in Figure 3c shows the temperature near contact B as a function of bias V_B. It is clear from these data that charge trapping will be facilitated selectively in the area between contact B and the finger contact due to the extremely high temperature there.

An important characteristic of a p−n junction is the creation of a photocurrent under light illumination. In photocurrent microscopy,[28−32] a focused laser spot is scanned over the sample, while the short-circuit photocurrent (taken at zero source−drain voltage) is measured as a function of the position of the incident laser spot and displayed as a spatial image. Figure 4 shows such a photocurrent microscopy image of an electrical stress-induced p−n junction, taken at a gate voltage of V_G = 2 V along with Raman line mapping. (Note that the Raman spectra in Figure 4c were taken at a gate voltage of V_G = 20 V as in Figure 3, so that the p-type doped region near the right contact appears undoped because the effects of gate voltage and trapped charges cancel out.) Importantly, the position of the photocurrent peak coincides with the junction position as determined by the Raman measurements. A photocurrent of about 30 nA is generated at an incident laser power of 100 μW. This corresponds to a photon responsivity of 3×10^{-4} A/W, which is very high for a one-atom thin layer, when compared to an equivalent thicknesses of bulk photodetectors.[29] We measure a width of the photocurrent peak of around 1 μm. Considering that this width is close to the resolution of the confocal setup (700 nm), while photocurrent microscopy is a nonconfocal technique, indicates that the

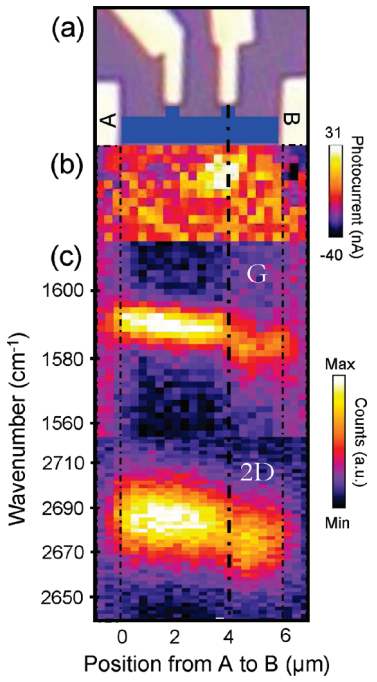

Figure 4. Photocurrent microscopy determines the position of the p−n junction. (a) Optical image of the electrically stressed graphene field-effect transistor. (b) Short-circuit photocurrent image (λ = 514.5 nm, V_G = 2 V, V_B = 0 V) of the p−n junction near the right finger contact. The junction was previously formed by stressing up to V_G = 20 V and V_B = 14 V and the finger contact acted as a heat sink. A photocurrent of 30 nA can be generated by an incident laser power of 100 μW. (c) Raman intensity plotted as a function of position (*x*-axis) and wavenumber (*y*-axis), measured at V_G = 20 V and V_B = 0 V, showing a discontinuity due to a step in the doping profile due to the previous stress. The position of the photocurrent is well-aligned with the step in the doping profile and the metal finger.

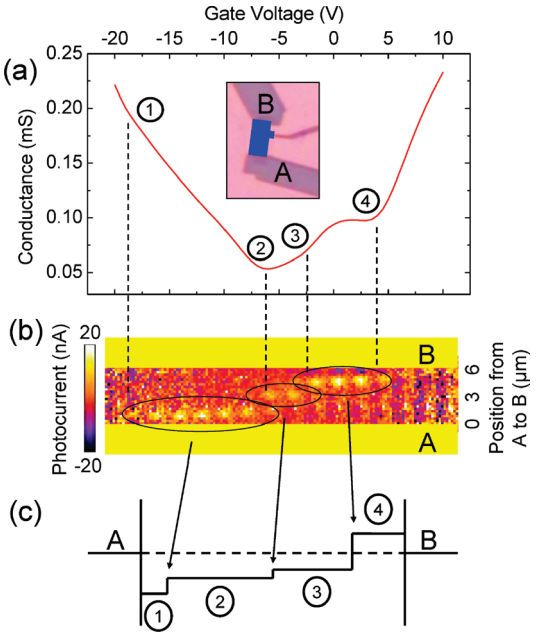

Figure 5. Photocurrent microscopy of a multiple junction graphene device. (a) Conductance *vs* gate voltage plot (V_A = −100 mV) of the device shown in the inset, after multiple electrical stress cycles with (i) V_G = −18 V, V_A = −10 V; (ii) V_G = −22 V, V_A = −10 V; (iii) V_G = −26 V, V_A = −10 V. Four CNPs can be identified at V_G = −18, −7, −3, and 4 V (indicated by numbers 1−4 and dotted lines). (b) Sequence of spatial photocurrent images (λ = 514.5 nm) for zero bias and gate voltages between V_G = −20 and 10 V in 2 V steps. Three areas with strong photocurrent (bright spots) can be identified at positions where differently doped graphene segments form p−n junctions. For gate voltages between two CNPs, the Fermi level lies between the energies of two adjacent segments, and a p−n junction is formed, exhibiting a photocurrent. (c) Extracted band-bending in the graphene device.

carriers have to be photoexcited in the immediate vicinity of the junction in order to produce a photocurrent. Carrier diffusion to the junction, where charge separation can take place, is limited in graphene by the short lifetime of photoexcited carriers.

The gate-voltage dependence of the photocurrent can give additional insight into the p−n junction properties and the origin of the photocurrent. For this, we electrically stressed another graphene field-effect transistor multiple times with varying gate voltages, leading to a device with four differently charged graphene segments and three junctions between them. Four dips in the $G-V_G$ characteristic can be identified in Figure 5a at V_G = −18, −7, −3, and 4 V, corresponding to CNPs of the four segments (Figure 5c). Generation of a photocurrent is limited to the gate-voltage range between V_G = −18 V and V_G = 4 V (Figure 5b). Moreover, each junction appears in the photocurrent data exactly at gate voltages between the two CNPs that correspond to the two segments forming the junction. This can be easily understood in a model where the photocurrent originates from the built-in electric fields.[14,28−30,32] At gate voltages between two CNPs, a junction behaves like a p−n junction, which produces a photocurrent. At other gate voltages, the junction becomes p−p$^+$ or n−n$^+$, which does not produce a photocurrent.

To accurately determine the abruptness of the p−n junctions, we can follow the movement of the photocurrent spot when the gate voltage is varied between the CNPs of two neighboring graphene segments. In an ideally abrupt junction, the photocurrent spot would be absolutely stationary during the gate-voltage sweep, while for graded junctions, it should move laterally because the Fermi level crosses the charge-neutrality point at different positions for each gate voltage. In this manner, we find that the first segment between CNPs 1 and 2 has a junction width of 500 nm, while the other two junctions are only about 200 nm wide. These values are consistent with the previous measurements of the doping and temperature profiles in similar junctions by Raman spectroscopy (Figures 2 and 3).

From the positions of the contacts and the three p−n junctions, we estimate the lengths of the four nanotube segments as L_1 = 0.6 μm, L_2 = 2.4 μm, L_3 = 1.8 μm, and L_4 = 1.2 μm. These lengths are associated with the

conductance at the corresponding CNPs. For example, the first graphene segment is quite short, and therefore, the first CNP at $V_G = -18$ V is quite shallow. Compared to that, the next two segments are much larger, and their corresponding CNPs are also much lower. This knowledge in combination with the gate-voltage range over which the p−n junctions are visible allows us to draw the band-bending in the device as shown in Figure 5c. The energies of the four segments are drawn according to $E \sim \sqrt{n} \sim (V_G - V_{CNP})^{1/2}$ for $V_G = 0$ V, and the lengths of the segments are taken from the positions of the three p−n junctions.

Notice also that the photocurrent has only one sign, contrary to what can be observed at graphene−electrode contacts[28−30,32] or single-layer/double-layer graphene junctions.[31] At a contact, the band-bending can be reversed because the Fermi level in the graphene under the contact is partially pinned while the Fermi level in the graphene channel can be gated n- or p-type. In contrast, the band-bending in the p−n junction cannot be switched to that of an n−p junction by a global backgate alone. The fact that there is only one sign of photocurrent at all gate voltages also suggests that thermoelectric contributions to a photocurrent[31] in graphene p-n junctions are small compared to the contributions of the built-in electric field, as demonstrated before in ref 14.

In conclusion, p−n junctions in graphene are realized by simultaneously applying high source−drain and gate biases. Raman maps of the 2D-band show that the graphene near the biased contact gets very hot during the electrical stress, while the area near the grounded electrode stays cold. Finger contacts can act as heat sinks that help to sustain the large temperature differences in the graphene. High local temperatures promote local charge trapping close to the oxide surface, which leads to a doped graphene segment even after the electrical stress has been removed. Subsequent Raman maps of the G-band indicate the accumulation of charges in the graphene starting at the previously biased electrode. Localized photocurrents due to the built-in electric fields at the induced p−n junctions coincide spatially with the doping steps detected by Raman. These optical measurements allow the reconstruction of the band-bending in electrically stressed devices.

METHODS

Graphene transistors are fabricated by micromechanical exfoliation of Kish graphite (Toshiba Ceremics). Metallic contacts (0.5 nm/20 nm/30 nm of Ti/Pd/Au) are formed on the graphene sheet by e-beam lithography and high-vacuum metal evaporation followed by hot acetone lift-off. The graphene channel, defined by reactive-ion etching of the undesirable graphene areas using oxygen plasma, is 6 μm long and 1 μm wide. The SiO_2 gate oxide thickness is 90 nm, facilitating good electrostatic field-effect gating of the transistor and junction. Samples are pumped for several days with a turbo pump near 10^{-6} Torr and annealed at 50 °C in vacuum before starting the measurements in order to remove adsorbates that dope the device and to bring the CNP close to 0 V. A schematic illustration of the vacuum chamber setup, in which the optical measurements are carried out as well, is shown in Figure 1a. Electronic feed throughs allow the application of a bias to the wire-bonded sample, and a sapphire window above the sample allows optical access *in situ*. Thus the sample stays in vacuum at all times. A 50× objective with numerical aperture of NA = 0.55 and long working distance is used to focus the laser with $\lambda = 514.5$ nm onto the sample. This provides a spot size of about 0.7 μm. Laser power levels on the sample are kept around 0.1 mW to avoid sample heating and to minimize changes in the $I-V_G$ characteristic. Note that some small shifts in the Dirac point due to the interaction of the light with trapped charges or dopants cannot entirely be avoided even at these low power levels. However, the trapping due to electrical stress is much stronger than the detrapping due to the light, and the Raman shifts due to the light-induced detrapping are negligible. Spatial Raman maps (one-dimensional line scans along the axis of the device) are obtained using a closed-loop piezo scanning mirror. Raman-scattered light is analyzed by a TRIAX Horiba JY 322 spectrometer with a liquid nitrogen-cooled Si CCD. A confocal pinhole is used to improve resolution and signal-to-noise ratio in the Raman measurements. The spectrometer line width is measured to be 4 cm^{-1} for a 1200 lines/mm grating. Relative spectral peak positions can be determined with better than 1 cm^{-1} resolution.

Throughout this paper, we electrically stress the devices with multiple drain-voltage sweeps from 0 V to a maximum drain voltage on the order of $|V_D| \sim 10-14$ V, increasing the gate voltage in small steps ~1 V for each drain-voltage sweep up to a maximum gate voltage V_G for the last sweep. The amount (and sign) of charge trapping in the oxide depends mainly on the maximum gate voltage during the electrical stress because the gate voltage lowers or increases the energy of the charge traps relative to the graphene Fermi level and makes the trap states available for filling or emptying in thermally assisted tunneling processes. The maximum drain voltage during the electrical stress needs to be large enough so that carriers can overcome tunneling barriers that separate the graphene channel from the charge traps. The tunneling barriers prevent the traps from neutralizing once the high electrical bias is removed and the altered potential landscape is then stable for at least as long as we measured the samples (several days) in vacuum. Both the maximum drain and gate voltages that were applied during the electrical stresses are provided in the figures. The slow variation of V_G ensures that the Fermi level in the graphene stays close to the altered Dirac point during all drain-voltage sweeps, and the charge trapping stays local.

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Supporting Information Available: Additional experimental details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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